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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/750,607	12/29/2003	James S. Song	TI-35767	8925

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TEXAS INSTRUMENTS INCORPORATED
P O BOX 655474, M/S 3999
DALLAS, TX 75265

EXAMINER	
SUGENT, JAMES F	
ART UNIT	**PAPER NUMBER**
2116	

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	03/13/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary	Application No.	Applicant(s)	
	10/750,607	SONG ET AL.	
	Examiner	Art Unit	
	James F. Sugent	2116	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *15 January 2007*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-23* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *1-12,21 and 22* is/are allowed.

6)☒ Claim(s) *13-17 and 23* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

This Office Action is sent in response to Applicant's Communication received January 15, 2007 for application number 10/750,607 originally filed December 29, 2003. The Office hereby acknowledges receipt of the following and placed of record in file: amended claims 1-23 (wherein claims 18-20 are canceled and claims 21-23 are new) are submitted for examination.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The factual inquiries set forth in *Graham* v. *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

Claims 13 are rejected under 35 U.S.C. 103(a) as being unpatentable over Chang et al. (U.S. Patent Publication No. 2003/0135836 A1) (hereinafter referred to as Chang) in view of

Nadeau-Dostie et al. (U.S. Patent Publication No. 2003/0146777 A1) (hereinafter referred to as Nadeau-Dostie).

As to claim 13, Chang disclose a method for balancing one or more clock signals in a clock tree having a clock distribution (paragraph 37), comprising: associating a first delay equalizer (48 and 49 at and above enable points C2 and C3) with at least one of a plurality of clock-gating cells (51 and 52) arranged in one or more levels in the clock tree (as shown in Fig. 8), the first delay equalizer operable to provide a balanced input clock signal to the clock-gating cell such that an output clock signal generated by the clock-gating cell is substantially balanced (paragraphs 36-39); a second delay equalizer (48 and 49 at and below enable points C2 and C3) operable to substantially balance the one or more clock signals (paragraphs 36-39); extracting a common clock distribution topology from the clock tree, the topology accounting for substantially all paths of the topology (paragraph 39); determining one or more clock paths (subtrees) to be balanced (Chang discloses determining which subtree paths need to be re-evaluated in order to properly balance the entire tree; paragraphs 43); analyzing any local clock paths that were left out of the common clock distribution topology (Chang discloses creating new endpoints in the clock subtree structures to properly evaluate and determine a balanced subtree by inserting new buffers to balance the delays; if the subtree is not balanced, a new endpoint is determined thus re-evaluated thus discovering new subtree branches that were left out of the evaluation process before; paragraphs 44-45); developing a local balancing strategy (subtree synthesis) for the local clock paths that were left out of the common clock distribution topology to determine one or more constraints for substantially balancing the local clock paths (Chang discloses balancing the lower subtrees and combining [synthesizing] all of the subtrees using two

techniques [zero-skew algorithm and subtree compression process] and re-evaluating until all subtrees are balanced; paragraphs 52-54); combining (synthesizing) the local balancing strategy (subtree analysis) with the common clock distribution (starting at the lower levels and working upward to all levels of the tree) to form a clock tree synthesis constraint to substantially balance the common clock distribution topology and the local clock paths in a substantially automatic process (Chang discloses balancing all levels of the tree using the CTS algorithm that automatically loops through a balancing/synthesizing process until the entire tree is synthesized; paragraphs 47-50).

Chang does not disclose the system: wherein the clock balancing system has multi-mode clock distribution; wherein the second delay equalizers are each associated with one or more clock-dividing and selection modules; wherein balanced clock signals associated with the second delay equalizers are between two or more functional modes; the common clock distribution topology accounting for substantially all of modes and clock-dividing paths of the topology; identifying a clock balance path, wherein the clock balance path is selected based on a requirement of a particular one of the two or more functional modes; and, determining each one of the one or more balanced clock paths includes a multi-mode dependant clock path, wherein the multi-mode dependant clock path includes the two or more functional modes.

Nadeau-Dostie teaches clock controlling circuitry (12) that balances multiple clocks (CLKA and CLKB): wherein the clock balancing system has multi-mode clock distribution (normal operating mode and test mode; paragraphs 5 and 39-43); wherein the second delay equalizers are each associated with one or more clock-dividing and selection modules (prescalars 64 and 66 in addition to MUXes 60, 62 and 68; paragraphs 21 and 22); and, wherein balanced

clock signals associated with the second delay equalizers are between two or more functional modes wherein each one of the one or more balanced clock paths includes a multi-mode dependant clock path, wherein the multi-mode dependant clock path includes the two or more functional modes (Nadeau-Dostie teaches the prescalars being selected dependent on the mode selection and the clock paths A, B' and B'' originated from CLKA and CLKB each comprise two or more modes that are selected via mux selection signals; paragraphs 20-23). Nadeau-Dostie further teaches identifying (via controllers 40, 42 and 44) a clock balance path, wherein the clock balance path is selected (via selection signals for mux's 46, 48, 50, 60, 62 and 68) based on a requirement of a particular one of the two or more functional modes (Nadeau-Dostie teaches the clock selection is based upon the receiving of enabling signals BIST_Enx from controller 40; paragraphs 20-23). Nadeau-Dostie has the additional feature of facilitating the distribution of clock signals to various clock domains and cores during both normal mode and testing mode which in turn will assist in the synchronization at all levels of the testing (paragraph 3, lines 21 thru paragraph 5).

It would have been obvious to one of ordinary skill of the art having the teachings of Chang and Nadeau-Dostie at the time the invention was made, to modify the system of Chang to include multi-mode clock balancing within the clock distribution wherein clock dividing circuits are used and balanced within the tree as taught by Nadeau-Dostie such that the extracting, balancing and combination processes of Chang account for multi-modal analysis and balancing. One of ordinary skill in the art would be motivated to make this combination of having multi-mode clock balancing within the clock distribution wherein clock dividing circuits are used and balanced within the tree in view of the teachings of Nadeau-Dostie, as doing so would give the

added benefit of facilitating the distribution of clock signals to various clock domains and cores during both normal mode and testing mode which in turn will assist in the synchronization at all levels of the testing (as taught by Nadeau-Dostie above).

As to claim 14, Chang in combination with Nadeau-Dostie taught the method in claim 13, as shown above. Chang further teaches the method wherein determining the one or more clock paths to be balanced comprises: determining an impact that balancing a particular clock path would have on overall clock tree balance and performance of a device associated with the clock tree (paragraph 43); determining whether the determined impact of the particular clock path exceeds a predetermined impact (paragraph 45, lines 1-8); and if it is determined that the determined impact of balancing the particular clock path exceeds the predetermined impact, determining that the particular clock path should be balanced (paragraph 45).

As to claim 15, it is directed to the method of steps set forth in claim 14. Therefore, it is rejected for the same basis as set forth hereinabove.

Claims 16 and 17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Chang in view of Nadeau-Dostie as applied to claim 13 above, and further in view of Albean et al. (U.S. Patent No. 5,517,109) (hereinafter referred to as Albean).

As to claim 16, Albean teaches a clock mode selection circuit (100) comprising one or more exclusive-NOR (XNOR) gates (140) (column 2, lines 12-26 and Fig. 1). Albean further teaches the XNOR gate receives an input clock signal on an input clock path (column 3, lines 25-36 and Fig. 1); receive a test mode signal (SELECT) on a test mode path (column 3, lines 25-65); and generate an output clock signal (CLOCK) on an output clock path based on an XNOR operation, a delay (via 135) from the input clock path to the output clock path being independent

of a delay from the test mode path to the output clock path (column 2, line 59 thru column 3, line 65). Albean has the additional benefit of decreasing the necessary time required to test a clock selection system (column 2, lines 1-10).

It would have been obvious to one of ordinary skill of the art having the teachings of Chang, Nadeau-Dostie and Albean at the time the invention was made, to modify method of Chang to include one or more XNOR gates to assist in clock selection as taught by Albean. One of ordinary skill in the art would be motivated to make this combination of including one or more XNOR gates in view of the teachings of Albean, as doing so would give the added benefit of decreasing the necessary time required to test a clock selection system (as taught by Albean above).

As to claim 17, Chang in combination with Nadeau- Dostie and in further view Albean taught the method in claim 16, as shown above. Albean further teaches the method wherein when the test mode signal received on the test mode path asserts test mode, the output clock signal generated by the XNOR gate comprises a non-inverted output clock signal (column 3, lines 25-36).

Claim 23 is rejected under 35 U.S.C. 103(a) as being unpatentable over Chang in view of Nadeau-Dostie as applied to claim 13 above, and further in view of Dean (U.S. Patent No. 5,553,276) (hereinafter referred to as Dean).

As to claim 23, Dean teaches a clock generation circuit (204) to synchronize clocks throughout a system (column 19, line 55 thru column 20, line 20). Dean further teaches determining which of the functional modes is most significantly impacted by the one or more clock signals (Dean teaches the system evaluating all of the possible mode selections delivering

selection signals to the clock generator 204 wherein the selection signals are further evaluated to determine how the selection will impact the system; column 61, lines 45-61). Dean has the added feature of including self-timed processing, in which dynamic, adaptive operation, efficient and flexible interfaces, low power consumption, and a wide environmental operating range are provided (column 1, lines 48-60).

It would have been obvious to one of ordinary skill of the art having the teachings of Chang, Nadeau-Dostie and Dean at the time the invention was made, to modify the method of Chang to include determining how the functional modes will impact the clock signals as taught by Dean. One of ordinary skill in the art would be motivated to make this combination of determining how the functional modes will impact the clock signals in view of the teachings of Dean, as doing so would give the added benefit of including self-timed processing, in which dynamic, adaptive operation, efficient and flexible interfaces, low power consumption, and a wide environmental operating range are provided (as taught by Dean above).

Allowable Subject Matter

Claims 1-12, 21 and 22 are allowed.

The following is a statement of reasons for the indication of allowable subject matter in re independent claims 1 and 7. Wang et al. (U.S. Patent No. 6,549,045 B1) teaches the limitations of: a delay equalizer for balancing clock signals in a clock tree, comprising: a register operable to: receive a divided input clock signal; receive a non-divided input clock signal; and generate a first output clock signal based on the received divided input clock signal and the received non-divided input clock signal, the first output clock signal being associated with a first

delay; a delay line operable to: receive the non-divided input clock signal; delay the non-divided input clock signal for a time substantially equivalent to the first delay associated with the first output clock signal; and generate a second output clock signal being associated with a second delay substantially equal to the first delay of the first output signal; and a multiplexer operable to: receive the first output clock signal and the second output clock signal; receive a select control signal indicating which of the first output clock signal or the second output clock signal to select; select either the received first output clock signal or the second output clock signal based on the select control signal; and generate the selected first output clock signal or second output clock signal as a substantially balanced third output clock signal. Cheung et al. (U.S. Patent No. 6,564,329 B1) further teaches the select control signal is programmable on the fly, and wherein the select control signal is constrained to avoid errors in clock distribution. Neither Wang nor Cheung teaches, either singularly or in combination, the limitation of "...wherein the select control signal transitions only when the first output clock signal and the second output clock signal have the same phase; ..." nor could it be found in further Examiner's search. Therefore, independent claims 1 and 7 in addition to dependent claims 2-6, 8-12, 21 and 22 are deemed allowable.

Response to Arguments

Applicant's arguments with respect to claims 13-17 and 23 have been considered but are moot in view of the new ground(s) of rejection.

The Applicant argues improper filing of Final Office Action submitted October 23, 2006 due to new the introduction of new art. However, the new art was introduced on the grounds of

amended independent claims. Therefore, Applicant's request for reconsideration of the finality of the rejection of the last Office action is not persuasive. To that end, the finality of that action is not withdrawn. Furthermore, the filing of the RCE, submitted January 15, 2007, deems the argument for withdrawal of finality moot.

5

Conclusion

Any inquiry concerning this communication or earlier communications from the Examiner should be directed to James Sugent whose telephone number is (571) 272-5726. The Examiner can normally be reached on 8AM - 4PM.

10 If attempts to reach the Examiner by telephone are unsuccessful, the Examiner's supervisor, Rehana Perveen can be reached on (571) 272-3676. The fax phone number for the organization where this application or proceeding is assigned is (571) 273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications 15 may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at (866) 217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated 20 information system, call (800) 786-9199 (IN USA OR CANADA) or (571) 272-1000.

James F. Sugent
Patent Examiner, Art Unit 2116
March 7, 2007

REHANA PERVEEN
SUPERVISORY PATENT EXAMINER
3/12/07